What is claimed is:

1. A power factor correction circuit comprising:

a power circuit comprising first and second input capacitors forming a bank node; first and second inductors, the first and second inductors inductively coupled, the first inductor connected to the first input capacitor and the second inductor connected to the second input capacitor; first and second switches, the first switch connected to the first inductor and the bank node, the second switch connected to the second inductor and the bank node; and an output circuit connected to the first and second inductors and the bank node, the output circuit operable to produce an output voltage;

a control circuit operable to monitor the output voltage and produce a switch signal at a switching frequency; and

a drive circuit coupled to the control circuit and the first and second switches, the drive circuit operable to operate the first and second switches based on the switch signal.

2. The power factor correction circuit of claim 1, wherein the drive circuit and control circuit are connected to a flying node, the flying node at a common voltage at the switching frequency.

3. The power factor correction circuit of claim 2, wherein the drive circuit is a high side driver.

4. The power factor correction circuit of claim 2, wherein the control circuit comprises a difference amplifier connected to the output circuit to measure an output circuit voltage, the difference amplifier rejecting the common voltage at the switching frequency and producing an output voltage based on the output circuit voltage.

5. The power factor correction circuit of claim 4, further comprising a third inductor, the third inductor inductively coupled to the first and second inductors and connected to the control circuit, and wherein the third inductor bucks the common voltage at the switching frequency.

6. The power factor correction circuit of claim 5, wherein the output circuit comprises:

first and second output capacitors, the first and second output capacitors connected to the bank node;

a first diode interposed between the first output capacitor and the first switch; and

a second diode interposed between the second output capacitor and the second switch.

7. The power factor correction circuit of claim 6, wherein the first and second switches are IGBT switches.

8. The power factor correction circuit of claim 6, wherein the first and second switches are MOSFET switches.

9. The power factor correction circuit of claim 6, wherein the first and second inductors are moderately coupled.

10. The power factor correction circuit of claim 2, wherein the drive circuit operates the first and second switches simultaneously.

11. The power factor correction circuit of claim 10, wherein the drive circuit comprises:

a first drive circuit providing a first drive signal for the first switch, the first drive signal referenced to the bank node; and

a second drive circuit providing a second drive signal for the second switch, the second drive signal referenced to the flying node.

12. The power factor correction circuit of claim 11, wherein the first and second drive circuits include first and second gate transformers, respectively.

13. The power factor correction circuit of claim 11, wherein the first and second switches are optical switching devices, and the first and second drive circuits are optically coupled to the first and second switches, respectively.

14. The power factor correction circuit of claim 10, further comprising a rectifier for receiving an input power signal and generating an output power signal, the rectifier coupled to the first and second input capacitors.

15. The power factor correction circuit of claim 14, wherein the first and second input capacitors are matched capacitors, and wherein the input power signal is substantially divided across the first and second input capacitors.

16. A power factor correction circuit comprising:

a power circuit comprising an input bank and a switched output bank, the input bank and the switched output bank symmetric about a bank node and connected to the bank node, the input bank operable to receive a rectified input power signal and the switched output bank operable to switch symmetrically about the bank node and generate an output power signal symmetrical about the bank node;

a control circuit coupled to the input bank and the switched output bank, the control circuit referenced to a flying node at a common voltage at a switching frequency, the control circuit operable to measure the input power signal and the output power signal and generate a switching signal at the switching frequency; and

a drive circuit coupled to the switched output bank, the drive circuit operable to receive the switching signal and generate a first drive signal referenced to the bank node and a second drive signal referenced to the flying node, the first and second drive signals causing the switched output bank to switch symmetrically about the bank node.

17. The power factor correction circuit of claim 16, wherein the input bank comprises:

first and second input capacitors connected to the bank node; and

first and second inductors, the first and second inductors inductively coupled, the first inductor connected to the first input capacitor and the second inductor connected to the second input capacitor.

18. The power factor correction circuit of claim 17, wherein the switched output bank comprises:

first and second switches, the first switch connected to the first inductor and the bank node, the second switch connected to the second inductor and the bank node;

first and second output capacitors, the first and second output capacitors connected to the bank node; and

first and second diodes, the first diode interposed between the first output capacitor and the first switch, and the second diode interposed between the second output capacitor and the second switch.

19. The power factor correction circuit of claim 18, wherein the control circuit comprises a difference amplifier connected to the switched output bank to measure an output bank voltage, the difference amplifier rejecting the common voltage at the switching frequency and producing an output voltage based on the output bank voltage.

20. The power factor correction circuit of claim 19, further comprising a third inductor, the third inductor inductively coupled to the first and second inductors and connected to the control circuit, and wherein the third inductor bucks the common voltage at the switching frequency.

21. The power factor correction circuit of claim 20, wherein the first and second switches are IGBT switches.

22. The power factor correction circuit of claim 20, wherein the first and second switches are MOSFET switches.

23. The power factor correction circuit of claim 18, wherein the drive circuit operates the first and second switches simultaneously.

24. The power factor correction circuit of claim 23, wherein the drive circuit comprises:

a first drive circuit providing a first drive signal for the first switch, the first drive signal referenced to the bank node; and

a second drive circuit providing a second drive signal for the second switch, the second drive signal referenced to the flying node.

25. The power factor correction circuit of claim 18, wherein the first and second input capacitors are matched capacitors, and wherein the input power signal is substantially divided across the first and second input capacitors.

26. A power factor correction circuit comprising:

a power circuit comprising an input circuit, a first switch, and a second switch; the input circuit symmetric about a bank node; the first switch and the second switch symmetrically coupled to the bank node and the input circuit; the input circuit operable to

receive a rectified input power signal and divide the rectified power signal evenly about the bank node when the first and second switches are in a closed state; and

a drive circuit coupled to the first and second switches, the drive circuit operable to receive a switching signal and generate a first drive signal referenced to the bank node and a second drive signal referenced to a flying node;

wherein the flying node is at a common voltage at a switching frequency.

27. The power factor correction circuit of claim 26, further comprising an output circuit symmetric about the bank node, the output circuit operable to generate an output power signal divided about the bank node.

28. The power factor correction circuit of claim 27, further comprising a control circuit, the control circuit coupled to the input circuit and the output circuit, the control circuit referenced to the flying node, the control circuit operable to measure the input power signal and output power signal and generate a switching signal at the switching frequency.

29. The power factor correction circuit of claim 28, wherein the control circuit comprises a difference amplifier connected to the output circuit to measure an output circuit voltage, the difference amplifier rejecting the common voltage at the switching frequency and producing an output reference voltage based on the output circuit voltage.

30. A power system comprising a plurality of power supply units ("PSUs"), each PSU having an output that is coupled to the output of other PSUs in the power system, each PSU comprising:

a power factor correction ("PFC") assembly for receiving an AC input and generating a first DC output, the PFC assembly comprising:

a power circuit comprising an input circuit, a first switch, and a second switch; the input circuit symmetric about a bank node; the first switch and the second switch symmetrically coupled to the bank node and the input circuit; the input circuit operable to receive a rectified input power signal and divide the rectified power signal evenly about the bank node when the first and second switches are in a closed state; and

a drive circuit coupled to the first and second switches, the drive circuit operable to receive a switching signal and generate a first drive signal referenced to the bank node and a second drive signal referenced to a flying node;

wherein the flying node is at a common voltage at a switching frequency;

a DC/DC converter assembly that is coupled to the PFC assembly, the DC/DC converter assembly receiving the first DC output and generating a second regulated DC output; and

a control assembly that is coupled to the DC/DC converter assembly, the control assembly being operative to monitor the DC/DC converter assembly output and in response thereto to provide control signals to the DC/DC converter assembly, the control assembly comprising,

a plurality of control assembly input circuits, the control assembly input circuits being operative to measure characteristics relating to the DC/DC converter assembly and operative to generate a measured characteristics output;

a signal processor having a signal path to the control assembly input circuits, the signal processor being operative to receive the measured characteristics output, perform computations wherein the measured characteristics output is used in the computations, and generate a signal processor output; and

a plurality of control assembly output circuits, the control assembly output circuits being operative to generate error signals based on the signal processor output.

31. A method of converting AC power to DC power in a converter circuit, comprising:

defining a bank node in a converter circuit;

defining a flying node in a converter circuit;

generating an bank voltage across the bank node and a pair of output terminals so that the bank node is at a half-bank voltage, the half-bank voltage approximately equal to one-half the magnitude of the bank voltage;

generating first and second states in the converter circuit;

changing the potential of the flying node by a magnitude equal to the half-bank voltage during a transition from the first state to the second state and during a transition from the second state to the first state.

32. The method of claim 31, wherein:

generating first and second states in the converter circuit comprises:

creating two symmetric converter topologies during the first state; and

releasing energy in each symmetric converter topology to maintain the bank voltage during the first state.

33. A system for converting AC power to DC power in a converter circuit, comprising:

means for defining a bank node in a converter circuit;

means for defining a flying node in a converter circuit;

means for generating an bank voltage across the bank node and a pair of output terminals so that the bank node is at a half-bank voltage, the half-bank voltage approximately equal to one-half the magnitude of the bank voltage;

means for generating first and second states in the converter circuit; and

means for changing the potential of the flying node by a magnitude equal to the half-bank voltage during a transition from the first state to the second state and during a transition from the second state to the first state.